

METHOD FOR FORMING DAMASCENE STRUCTURE UTILIZING PLANARIZING MATERIAL COUPLED WITH DIFFUSION BARRIER MATERIAL

Abstract

This invention relates to the manufacture of dual damascene interconnect structures in integrated circuit devices. Specifically, a method is disclosed for forming a single or dual damascene structure in a low-k dielectric thin film utilizing a planarizing material and a diffusion barrier material. In a preferred dual damascene embodiment of this method, the vias are formed first in the dielectric material, then the planarizing material is deposited in the vias and on the dielectric material, and the barrier material is deposited on the planarizing material. The trenches are then formed lithographically in the imaging material, etched through the barrier material into the planarizing material, and the trench pattern is transferred to the dielectric material. During and following the course of these etch steps, the imaging, barrier and planarizing materials are removed. The resultant dual damascene structure may then be metallized. With this method, the problem of photoresist poisoning by the interlevel dielectric material is alleviated.